ABSTRACT

A field programmable gate array (FPGA) device includes a high-speed serializer/deserializer (SERDES). The field programmable gate array allows programmable built-in testing of the SERDES at operating speeds. A digital clock manager circuit allows clock signals coupled to the SERDES to be modified during the test operations to stress the SERDES circuit. The logic array of the FPGA can be programmed to generate test patterns and to analyze data received by the SERDES circuit. Cyclic redundancy check (CRC) characters, or other error checking characters, can also be generated using the logic array. During testing, the FPGA can perform extensive tests on the communication circuitry and store the results of the testing. An external tester can read the results of the test without substantial test time or complicated test equipment. After testing is complete, the device may be re-programmed to perform the end-user function, adding zero cost to the device for test implementation.